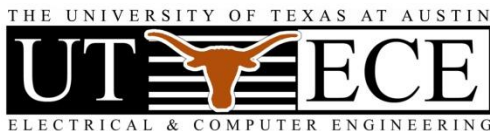


Hermes: An Integrated CPU/GPU Microarchitecture for IP Routing

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Yubei Chen[‡]

*** Electrical and Computer Engineering
University of Texas at Austin**



**‡ Institute of Microelectronics
Tsinghua University**



Motivation: IP Routing

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- Challenges in IP Router design

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 - Internet traffic is still increasing

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**Throughput &
QoS!**

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**Throughput &
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- New network services and protocols keep appearing

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**Throughput &
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Programmability

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- Traditional router solutions

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 - Hardware Routers: ASIC, Network Processors
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- How about GPUs?

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 - Hardware Routers: ASIC, Network Processors
 - PC based Software Routers
- How about GPUs?
 - High computing power

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- Hardware Routers: ASIC, Network Processors
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- How about GPUs?

- High computing power
- Mass market with strong development support

GPU based Software Router

- Related Work
 - Smith et al. [ISPASS2009]
 - Mu et al. [DATE2010]
 - Han et al. [SIGCOMM2010]

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- CPU/GPU communication overhead hurts overall throughput

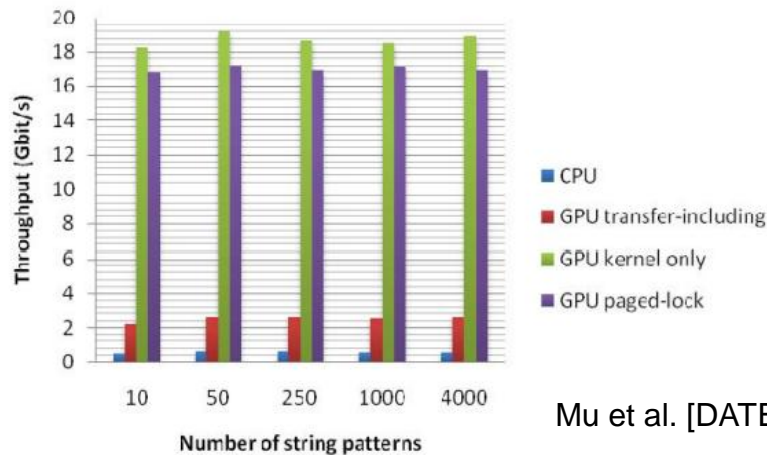
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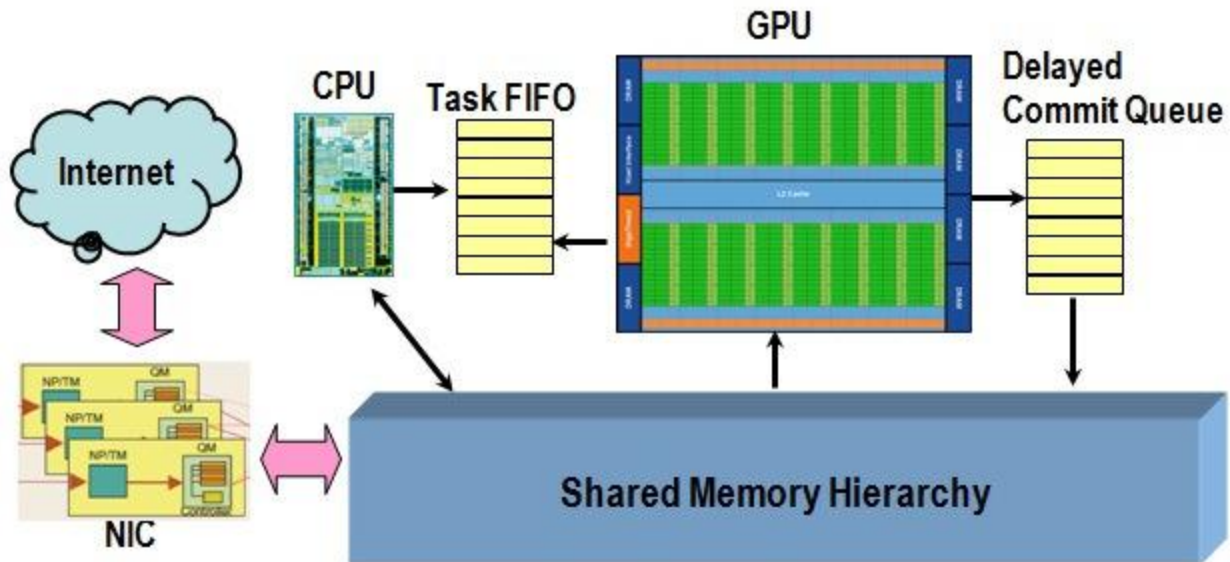
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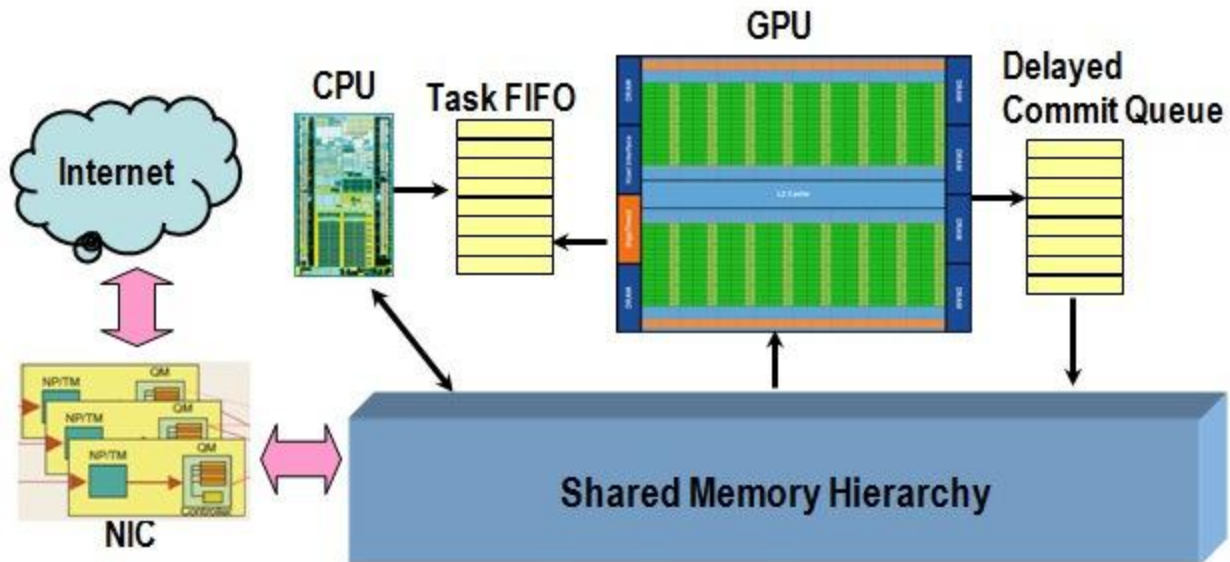
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Worst case delay:
 $batch_transfer_granularity / line_card_rate$

Hermes Microarchitecture

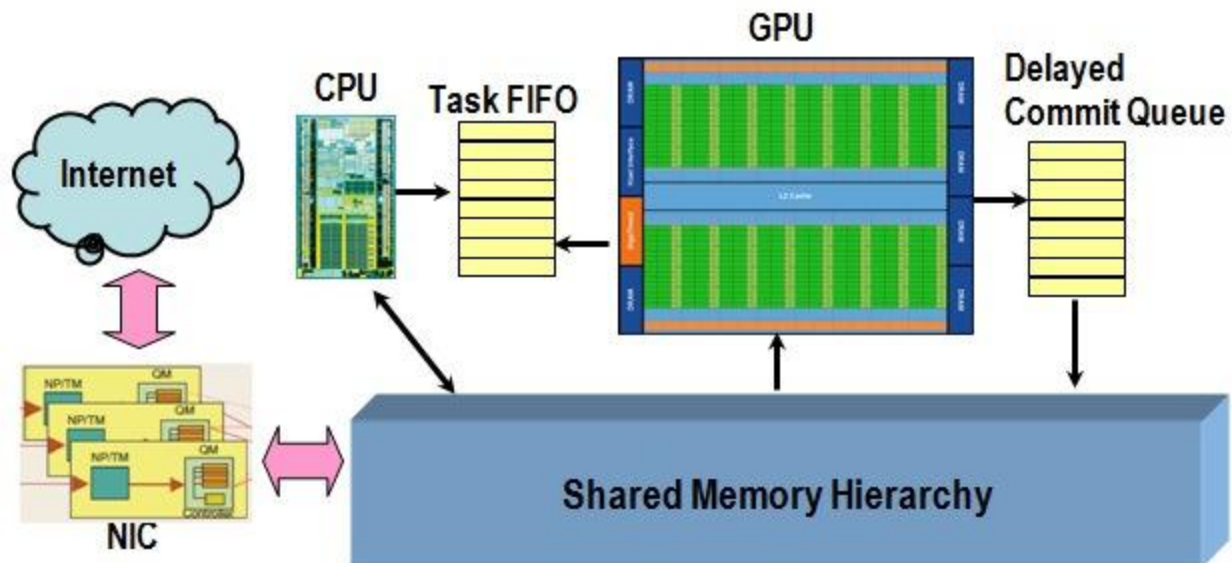


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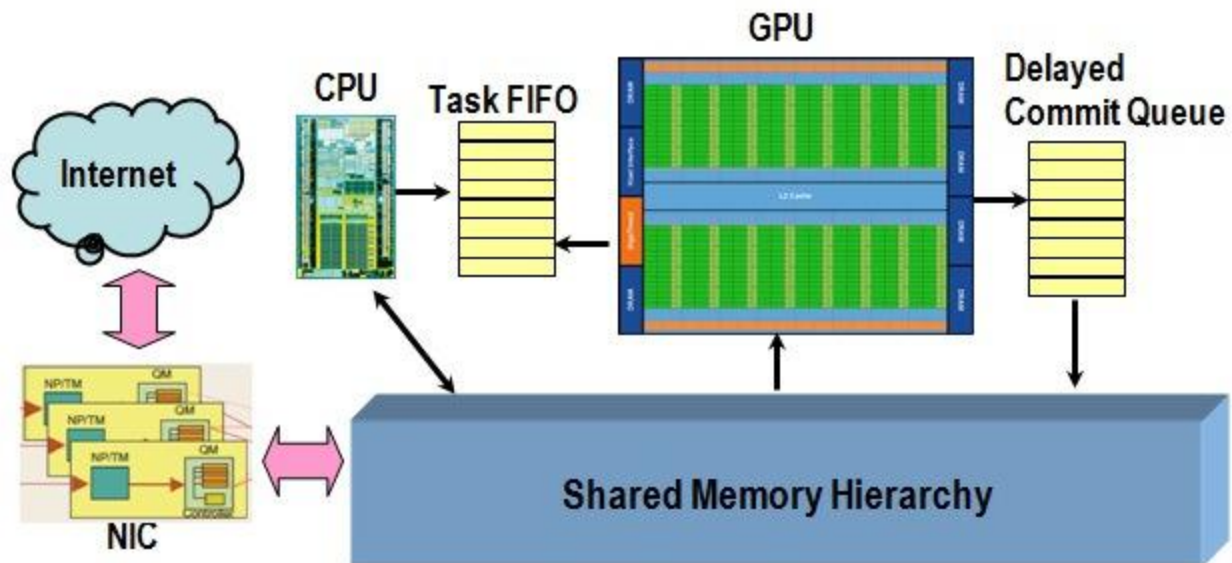
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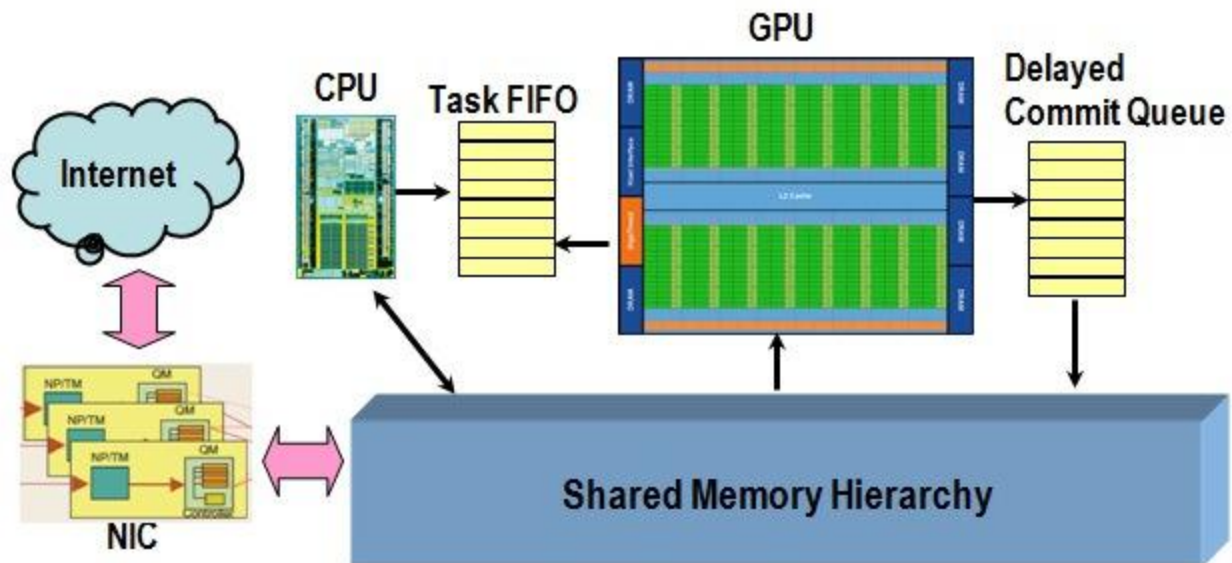
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Hermes Microarchitecture



- Throughput wins!
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 - Adaptive warp scheduler through Task FIFO and DCQ

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- Why?

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 - ❑ Avoid consistency issues in shared memory systems

Adaptive Warp Scheduler

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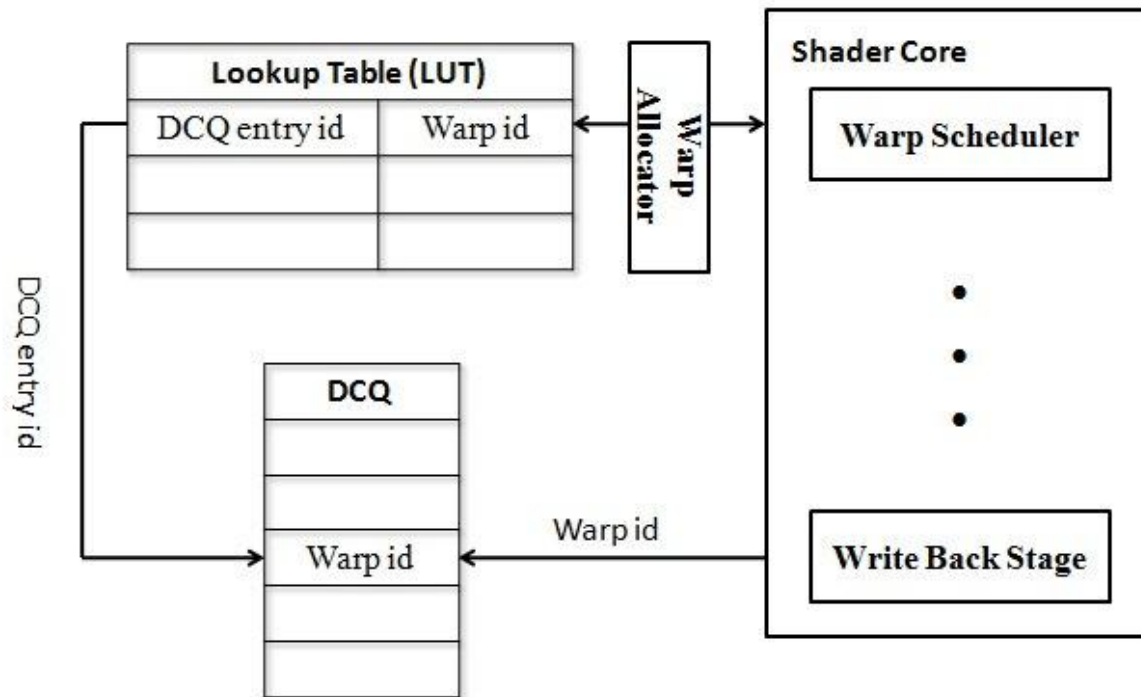
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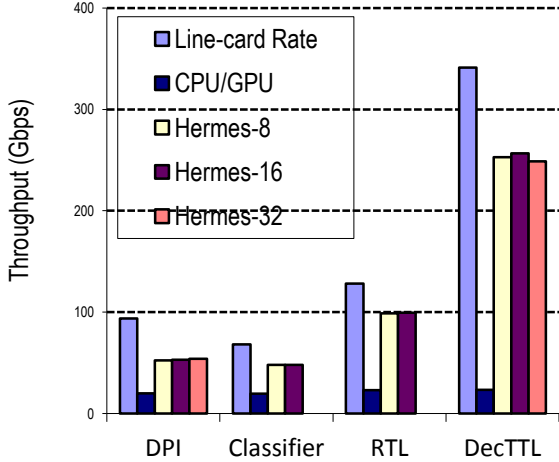
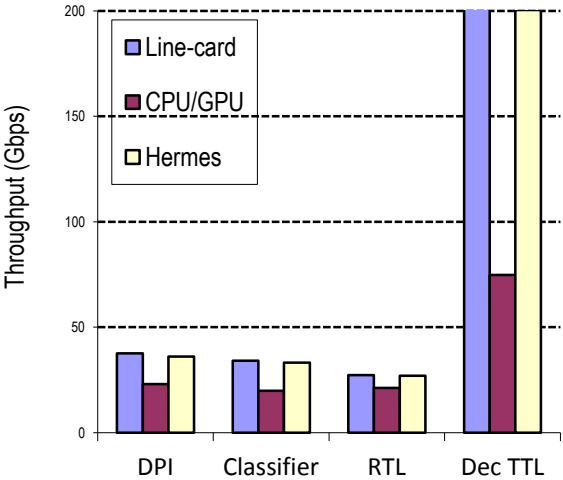
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- Maximally allowed concurrent warps (MCW) per core
 - They compete for hardware resources
 - They affect the updating/fetching frequency

Evaluations

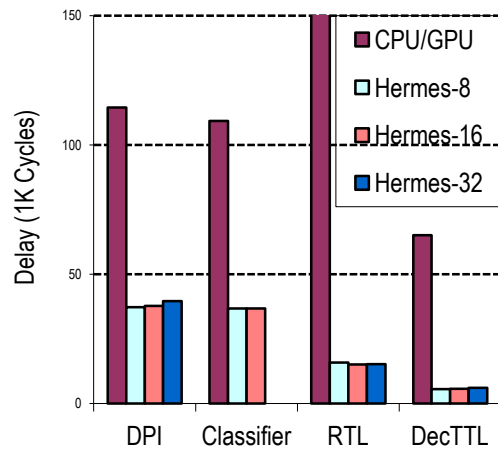
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Throughput



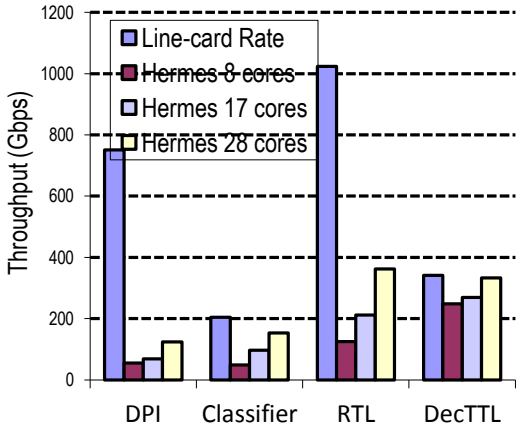
Evaluations

■ Delay



Evaluations

- Scalability



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Come to my poster to learn more!